Q-1 Describe the use of Cache memory? What are Hit and Miss states corresponding to cache memory?

Q-2 Write down the mapping types used in Cache Memory?

Q-3 Describe the types of Locality of reference used in Cache Memory?

Q-4 Consider a memory system with the following parameters:

Tc = 100 ns , Cc = 10^{-4} $/bit , Tm = 1200 ns, Cm = 10^{-5} $/bit

a. What is the cost of 1 Mbyte of main memory? b. What is the cost of 1 Mbyte of main memory using cache memory technology? c. If the effective access time is 10% greater than the cache access time, what is the hit ratio H?

Q5 Explain memory performance trade-off among cost, capacity and access time with example.

Q6 Differentiate between SRAM and DRAM memory chips.

Q7 Explain different memory access methods with an example for each of them.

[All numerical questions should be solved using proper steps and if possible use diagrams.]

Q8. An 8KB direct-mapped write-back cache is organized as multiple blocks, each of size 32-bytes. The processor generates 32-bit addresses. The cache controller maintains the tag information for each cache block comprising of the following. 1 Valid bit, 1 Modified bit as many bits as the minimum needed to identify the memory block mapped in the cache. What is the total size of memory needed at the cache controller to store meta-data (tags) for the cache?

Q9. A computer has a 256 KByte, 4-way set associative, write back data cache with the block size of 32 Bytes. The processor sends 32-bit addresses to the cache controller. Each cache tag directory entry contains, in addition, to address tag, 2 valid bits, 1 modified bit and 1 replacement bit. Calculate the number of bits in the tag field of an address? Calculate the size of the cache tag directory?

Q10. Consider a 4-way set-associative cache (initially empty) with total 16 cache blocks. The main memory consists of 256 blocks and the request for memory blocks is in the following order: 0, 255, 1, 4, 3, 8, 133, 159, 216, 129, 63, 8, 48, 32, 73, 92, 155. Which one of the following memory block will NOT be in cache if LRU replacement policy is used?

A) 3

(B) 8

(C) 129

(D) 216

Q11. Consider a 4-way set associative cache consisting of 128 lines with a line size of 64 words. The CPU generates a 20-bit address of a word in main memory. The number of bits in the TAG, LINE and WORD fields are respectively:

Q12. Given page reference string: 1,2,3,4,2,1,5,6,2,1,2,3,7,6,3,2,1,2,3,6 and the frame size is 4, calculate the number of page faults for LRU, FIFO and Optimal page replacement algorithm.

Q13. A 4-way set-associative cache memory unit with a capacity of 16 KB is built using a block size of 8 words. The word length is 32 bits. The size of the physical address space is 4 GB. The number of bits for the TAG field is ?